Today's Date: 7/17/2000

DB Name	Query	Hit Count	Set Name
USPT	((memory with access$) same (only with add$ offset$))	0	L15
USPT	((memory with access$) same (only with increment$ offset$))	0	L14
USPT	l10 and ((increment$) with (offset$) with only)	15	L13
USPT	l10 and ((increment$) with (offset$))	505	L12
USPT	l10 and (increment$ same (offset$))	1038	L11
USPT	memory.ab.	69702	L10
USPT	l6 and (add$ with displacement$)	0	L9
USPT	l6 and (add$$ with displacement$)	0	L8
USPT	l6 and (increment$ with displacement$)	0	L7
USPT	4155119.pn.	1	L6
USPT	l1 and (page same (increment$ with offset$))	11	L5
USPT	deward$.in.	7	L4
USPT	l1 and deward$.in.	1	L3
USPT	l1 and (decoder) and (register adj file) and vliw	100	L2
USPT	((712/$)!.CCLS.)	5885	L1

WEST

Your wildcard search against 2000 terms has yielded the results below

Search for additional matches among the next 2000 terms

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Search Results - Record(s) 1 through 10 of 15 returned.

☐ 1. Document ID: US 5886708 A

L13: Entry 1 of 15 File: USPT Mar 23, 1999

DOCUMENT-IDENTIFIER: US 5886708 A
TITLE: Graphic processor and a bit-built method applied therein

ABPL:
In order to realize a high-speed bit-built processing for superimposing pixel data of an image on to a video-memory, only substantial pixel data having color values different from a designated transparent color of a line of the image are stored in a line buffer (109) together with offset values of .chi.-addresses in the line of the substantial pixel data stored in a offset buffer (110). A memory controller (111) reads out the substantial pixel data from the line buffer in order, and writes them in a video memory (112) at a line according to writing addresses calculated by a writing address generator (106) referring to the offset values stored in the offset buffer corresponding to the substantial pixel data.

DEPR:
When the discrimination result 122 shows a transparent pixel, the buffer controller 104 only increments offset value 131 in the offset counter 105, the line buffer 109 and the offset buffer 110 taking no action.

DEPR:
Here, the buffer controller 504 only increments the offset value 531 in the burst counter 505, and leaves writing address 530 for the line buffer 509 and the offset buffer 510 left not revised, when the discrimination result 522 shows a transparent pixel, while it initializes the offset value 531 to `1` and increments the writing address for the line buffer 509 and the offset buffer 510, when the discrimination result 522 shows the pixel data 541 have other value than the transparent color 521. So, the offset value 531 in the burst counter 505, initial value thereof being `1`, is incremented when data of a transparent pixel are read out from the video memory 512, and it is reset to `1` when data of a substantial pixel are read out.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 2. Document ID: US 5819056 A

L13: Entry 2 of 15 File: USPT Oct 6, 1998

DOCUMENT-IDENTIFIER: US 5819056 A
TITLE: Instruction buffer organization method and system

ABPL:
Variable-length instructions are prepared for simultaneous decoding and execution of a plurality of instructions in parallel by reading multiple variable-length instructions from an instruction source and determining the starting point of each instruction so that multiple instructions are presented to a decoder simultaneously for decoding in parallel. Immediately upon accessing the multiple variable-length instructions from an instruction memory, a predecoder derives predecode information for each byte of the variable-length instructions by determining an instruction length indication for that byte, assuming each byte to be an opcode byte since the actual opcode byte is not identified. The predecoder associates an instruction length to each instruction byte. The instructions and predecode information are applied to an instruction buffer circuit in a memory-aligned format. The instruction buffer circuit prepares the variable-length instructions for decoding by converting the instruction alignment from a memory alignment to an instruction alignment on the basis of the instruction length indication. The instruction buffer circuit also assists the preparation of variable-length instructions for decoding of multiple instructions in parallel by facilitating a conversion of the instruction length indication to an instruction pointer.

DEPR:
In this manner, only an occasional increment of a few bits furnishes memory space conservation of a typical offset list method without performing a time-consuming addition operation. This technique advantageously allows for fast traversal of a list while reducing the space consumed to store each pointer.

☐ 3. Document ID: US 5621775 A

L13: Entry 3 of 15 File: USPT Apr 15, 1997

DOCUMENT-IDENTIFIER: US 5621775 A
TITLE: Device for justifying a digital bit stream at regular intervals

ABPL:
A digital bit stream from a first synchronous link is timed by a first clock and is to be sent over a second synchronous link timed by a second clock. A device for justifying the bit stream at regular intervals includes a buffer memory. Respective pointers supply buffer memory write and read addresses. A value indicating how full the buffer memory is is calculated and compared to first and second threshold values to produce a justification command signal. The first and second variable threshold values are determined according to the phase difference between the header of a row received from the first link and the header of a row sent at the same time on the second link. The device finds an application in gateways at the input of and in telecommunication networks using the synchronous digital hierarchy.

DEPR:
When the transient event which has caused the filling of the memory 12 is terminated, the processor 31 detects that the value .DELTA.P is now below the highest threshold value it reached during the transient. It starts a timer. When it registers that this event has lasted a duration T.sub.0 it changes the values of the parameters m1 and m2 in a predetermined sequence which is dependent only on time: every T.sub.1 seconds it increments the value of m1 by one unit; it then increments the value of m2 by one unit with an initial offset of T.sub.1 /2, and thereafter at regular intervals of T.sub.1 seconds, to revert to the initial values m1=16 and m2=16 in order to reduce the bandwidth of the filter 7'. Offsetting the incrementing of m1 and m2 reduces the phase jitter produced by changing the characteristic of the filter, corresponding to each change of value of m1 or m2.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw. Desc | Image

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☐ 4. Document ID: US 5502797 A

L13: Entry 4 of 15 File: USPT Mar 26, 1996

DOCUMENT-IDENTIFIER: US 5502797 A
TITLE: Apparatus with flash memory control for revision

ABPL:
Printer (1) receives revised operating code in flash memory (19). To preserve offset adjustment unique to the printer, the values in new operating code are compared with those in the previous code, and new offsets preserving the previous offsets are stored in permanent memory (21). The use of permanent memory is minimized by basing the calculation on changes from start of production.

BSPR:
No such revision addresses the preservations of earlier inputs specific to each apparatus. Such inputs are typically "fine tuning" information applied by skilled technicians in the factory or during maintenance, or inputs made by a skilled operator to satisfy the personal requirements and preferences of the operator. In the preferred embodiment of this application, such inputs are margin adjustments of the printer. Each printer, although within tolerances, has a slightly different overall operation. Accordingly, provision has been made in the control system to enter offset instructions to revise the margins from those which are nominally specified by the standard code. Thus, a factory technician will view actual printing and enter data specifying the amount of offset from what is seen. Each offset increment will be a small, predetermined amount and the amount of offset will typically be only a few of such units. However, the offset will differ for each printer because of the subtle differences between two nominally identical printers.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 5. Document ID: US 5438509 A

L13: Entry 5 of 15 File: USPT Aug 1, 1995

DOCUMENT-IDENTIFIER: US 5438509 A
TITLE: Transaction processing in a distributed data processing system

ABPL:
Nonvolatile memory is used extensively to increase system reliability and data integrity by reducing the chances of data loss due to a system shutdown. Data is stored to nonvolatile memory before pointers to the data are modified to eliminate problems due to pointers pointing to nonexistent data.

DEPR:
If the count is not equal to zero, one or more attribute-only fields exist and at 82 the count is saved. At 84 the index offset is incremented to the first attribute-only field. At 86 a check is then made to determine if the attribute pointed to by the offset index matches the attribute passed in the function call.

DEPR:
If the attributes do not match, at 90 the index offset is incremented to the next attribute-only field and at 92 the saved count is decremented by one. At 94 the count is compared to zero. If the count is zero, the end of the attribute only fields has been reached and at 96 the attribute offset is set to zero indicating to the application that the attribute was not found. The function then returns from the call.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 6. Document ID: US 5357276 A

L13: Entry 6 of 15 File: USPT Oct 18, 1994

DOCUMENT-IDENTIFIER: US 5357276 A
TITLE: Method of providing video on demand with VCR like functions

ABPL:
A near video on demand time shifting feature for a subscriber terminal emulates the video cassette recorder functions of pause, fast forward, and rewind for a NVOD service subscription. The subscriber terminal stores global transactions concerning NVOD events in an event portion of memory. The subscriber terminal provides an on screen display feature for assisting in ordering the NVOD service and a user interface which provides the functions of pause, fast forward and rewind. When viewing a NVOD event, if the subscriber selects the pause function, the subscriber terminal causes a pause on screen display to be viewed for one time increment. After the elapse of the time increment, the subscriber terminal will tune the channel of the next showing which is one time increment earlier than that presently viewed. If the subscriber selects the rewind function, the subscriber terminal will tune the channel of the next showing which is one time increment earlier than that presently viewed. If the subscriber selects the fast forward function, the subscriber terminal will tune the channel of the previous showing which is one time increment later than that presently received.

BSPR:
These previous systems allow the ordering of one event, at a predetermined time, which the broadcaster and the cable operators have agreed upon. If the subscriber is unavailable at that time or does not have a time shifting device such as a video cassette recorder (VCR), then the event will be missed with the loss of consumer satisfaction and cable operator revenue. To answer the need for allowing the subscriber more flexibility of when to order a pay-per-view event, the industry has now initiated programming termed near video on demand (NVOD). In the NVOD programming, the program event, for example a first run movie, is broadcast continuously on a single channel or multiple channels. This allows the subscriber much greater flexibility in selecting the time that he wants to either record or watch the particular program event. To increase this flexibility the event can be duplicated on several channels where the starting time of the event on each channel is offset by predetermined increment of time. Depending upon the number of channels and the length of the event, the subscriber will have to wait only one offset time increment until the program event next starts on an adjacent channel. Increasing the number of channels reduces the amount of time that a subscriber has to wait until the start of the program event and increases his satisfaction with the service. As an example, if the program event is one hour long, and there are four channels, and the start time of the program event on each channel is equally offset, then the subscriber will at most wait 15 minutes to the start of the next broadcast of the event.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw. Desc | Image

☐ 7. Document ID: US 5257061 A

L13: Entry 7 of 15 File: USPT Oct 26, 1993

DOCUMENT-IDENTIFIER: US 5257061 A
TITLE: Range finder for passive-type autofocusing device

ABPL:
A range finder circuit for a passive-type autofocusing device includes three line photosensors. Secondary differences of their output signals and zero-cross points of these secondary differences are computed and detected so long as these zero-cross points are those appearing when primary differences derived from computation of the secondary differences have absolute values larger than a predetermined value. The range to the scene is computed based on the amount of shifting of these signals into coincidence so that substantially no erroneous range finding occurs even when two objects composing the scene overlap each other. In a preferred embodiment also, signals from pixels of each photosensor are smoothed so that no erroneous range finding occurs even when the scene has on the surface thereof a fine repetitive pattern. The range finder circuit also responds to the output signals of the sensors to initiate write-in of zero-cross point data into associated zero-cross memory circuits which can be electrically position-adjusted so that the range to the scene can be computed substantially without error even when there is a certain error involved in mounting of the photosensors.

DEPR:
Luminance information on the scene to be photographed is written into and read out from the memory circuits by following the same steps of routine as in Embodiment 3.2. Specifically, the luminance information is written into the respective zero-cross memory circuits 14, 24, 34 under the pre-offset condition in order that the installation errors of the photosensors 10, 20, 30, if any, may be effectively compensated. Thus, under such pre-offset condition, the count signals (COUNTER 1) are applied from the first counter 50 not only to the address computing circuits 25, 35 but also to the central memory circuit 14 with successive increment, and the luminance data for the respective pixels are stored at the addresses given by the following equations:

☐ 8. Document ID: US 5185681 A

L13: Entry 8 of 15 File: USPT Feb 9, 1993

DOCUMENT-IDENTIFIER: US 5185681 A
TITLE: Thermal offset compensation for high density disk drives

ABPL:
A thermal offset compensation system is provided for use in a computer disk drive unit have a dedicated servo surface on one of a plurality of memory storage disks. The disk drive unit has a plurality of electromagnetic heads displaced as a group relative to respective storage surfaces on the disks to read and/or write data in concentric tracks. One of the heads comprises a servo head for reading servo data prerecorded onto the dedicated servo surface to align the remaining heads relative to corresponding cylinders of data tracks. Thermally induced offsets of the data heads relative to the servo head are measured on one or more calibration cylinders located in the inner and outer guard bands of each storage surface. The average offset of the data heads, taken collectively, is determined and subsequently compensated-for when any data head is utilized to read or write data on a selected track. The thermal compensation offset is determined during a spin-up operation of the disk drive unit, and then periodically thereafter upon receipt of any host command by the disk drive unit.

BSPR:
Following the initial calibration, the offset of each data head relative to the inner and outer guard band calibration cylinders is measured periodically. In particular, the offset relative to a calibration cylinder is measured only after the expiration of a predetermined time period and upon receipt of a host command by the disk drive unit. The offset applied to the data heads is changed only when the average offset changes at least by the minimum incremental unit value.

CLPR:
7. A method as set forth in claim 5, wherein with respect to the step of periodically measuring the offset of each data head relative to the inner or outer guard band calibration cylinders after the initial average offset of the data heads has been determined, such subsequent measurement of the offset occurs only after the expiration of a predetermined time period and upon receipt of a host command by the disk drive unit, wherein the average offset of the data heads is re-determined and applied in shifting the data heads relative to the selected cylinder to null the average offset determined, only when the average offset changes at least by the minimum incremental value.

CLPV:
determining a minimum incremental unit value for collectively adjusting the data heads during the shifting step, wherein the average offset of the data heads is re-determined and applied to the data heads relative to the selected cylinder to null the average offset determined, only when the average offset changes at least by the minimum incremental unit value; and

CLPV:
periodically measuring the offset of each data head relative to the inner or outer guard band calibration cylinders after the initial average offset of the data heads, taken collectively, has been determined, wherein such subsequent measurement of the offset occurs only after the expiration of a predetermined time period and upon receipt of a host command by the disk drive unit, wherein the average offset of the data heads is re-determined and applied in shifting the data heads relative to the selected cylinder to null the average offset determined, only when the average offset changes at least by the minimum incremental value; and

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw. Desc | Image

☐ 9. Document ID: US 4785415 A

L13: Entry 9 of 15 File: USPT Nov 15, 1988

DOCUMENT-IDENTIFIER: US 4785415 A
TITLE: Digital data buffer and variable shift register

ABPL:
A combination FIFO buffer and programmable shift register having asynchronous input and output capabilities comprises a three stage system which synchronizes the incoming data stream with the memory input clock, buffers the incoming data stream and provides a variable delay for the data. The digital data stream from an input device is received by an input synchronizer having its input clocked at the clock rate of the input device clock and its output clocked at a higher internal clock rate. The data is written into two FIFO buffers, a master and a slave. The master buffer controls the read and write addresses of both buffers, so that the write address of the buffers advances only when valid data is written into the buffers, and the read address advances only when data is read out of the buffers. The slave buffer can be programmed with an offset in its read address, so it operates as a delay buffer. The data is read out of the buffers into an output synchronizer, having its input clocked at the internal clock rate its output clocked at the clock rate of the memory control.

CLPV:
a read address counter having its initial count offset from the initial count of the write counter by said programmable number, clocked by the read phase of the internal clock signal and incremented only when the output data valid signal is present, having an output connected to the random access memory to control the second address.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw. Desc | Image

☐ 10. Document ID: US 4702698 A

L13: Entry 10 of 15 File: USPT Oct 27, 1987

DOCUMENT-IDENTIFIER: US 4702698 A
TITLE: Digital radar generator

ABPL:
A radar return image for display on a cockpit CRT is generated by selectively accessing terrain data compressed and stored in a digital map data base and processing that data to artificially simulate a radar return image pattern on a cockpit display which effectively corresponds that which would otherwise be provided by conventional T/R equipment. Since the compressed data base contains information representative of both the elevation and cultural features of the terrain at map locations that are capable of being intercepted by the aircraft's radar beam, this data may be subjected to signal processing functions to establish pixel intensity control signals by way of which a radar image of a cockpit CRT display is generated. This signal processing and control system includes system functional components for establishing the simulation of the effect of a radar beam having a prescribed beam width, slant-angle, and field of scan and controllably accessing the stored terrain map data from memory for establishing a pixel display data base in accordance with which the pixels of the cockpit radar display are intensity-modulated.

DEPR:
In order to generate X and Y address pairs for the respective points along individual rays of the radar sweep pattern, the X and Y component values referenced above in connection with FIG. 3 are added to the start point values supplied over links 33X and 33Y to multiplexers 171 and 181. At the beginning of an incrementing of data points along a respective ray, each of multiplexers 171 and 181 couples the start values over links 172 and 182, respectively, through adders 173 and 183 to registers 193 and 196. Thus, the initial address is the location of the observer or aircraft. The actual start point of a data point along the ray will depend upon the ray of interest and the increment value for that ray at the start point. For example, for ray (i+1), as shown in FIG. 3, the start point (or data point DP(i+1).sub.1) is displaced from the observer by the value .DELTA.R/2. This offset is supplied by each of offset PROMs 174 and 184 and added to the start point supplied over each of links 33X and 33Y in adders 173 and 183. The value is then stored in registers 193 and 196 in response to an address clock supplied over link 201. Thus, the X address and Y address supplied over links 202 and 203 for ray (i+1) will specify data point DP(i+1).sub.1 in terms of its .DELTA.X and .DELTA.Y values. Thereafter, unitary offset values for the successive data points along ray (i+1) are added to the contents of registers 193 and 196 as the contents of these registers are fed back through multiplexers 171 and 181 to adders 173 and 183. In other words, the contents of registers 193 and 196 are successively incremented by adding thereto the respective .DELTA.X and .DELTA.Y increment values from PROMs 161 and 162 which are coupled through multiplexers 175 and 185 by passing offset PROMs 174 and 184, which offset PROMs are used initially only for the starting data points. Thus for successive data points DP(i+1).sub.2, DP(i+1).sub.3 etc., corresponding X and Y addresses of these data points will be generated. These address values are supplied to square address unit 43 shown in FIG. 9.

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Your wildcard search against 2000 terms has yielded the results below

Search for additional matches among the next 2000 terms

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Search Results - Record(s) 11 through 15 of 15 returned.

☐ 11. Document ID: US 4594682 A

L13: Entry 11 of 15 File: USPT Jun 10, 1986

DOCUMENT-IDENTIFIER: US 4594682 A
TITLE: Vector processing

ABPL:
A cache memory, intermediate a CPU and a main memory, is employed to store vectors in a cache vector space. Three vector address operand registers are employed for reading vector operand elements from said cache memory and for writing results of vector operations back into cache memory. A data path from the cache memory allows vector operand elements to be written into selected local storage registers, and a path from the local storage registers to the cache memory includes a buffer. This apparatus allows overlapped reading and writing of vector elements to minimize the time required for vector processing.

DEPR:
In accordance with the invention, the cache 10 is used as a convenient space for implementing vector registers. For purposes of this description, the cache 10 is assumed to take one machine cycle to read data and 11/2 cycles to write data; the write consisting first of a cache read followed by a cache write modifying the data that was just read. In accordance with the invention, multiple element vector registers are mapped into the cache vector space such that an operand address register may be used to denote a particular vector register, and an offset register may be used to access consecutive elements of the vector register. See for example, FIG. 4 which is a memory map of cache 10, showing it divided into vector space 11 and scalar space 12. Plural vector registers are mapped into the vector space 11. FIG. 4 shows three such vector, registers one for each of vector operands 1, 2 and 3. Those skilled in the art will realize that many more than the three illustrative vector registers may be mapped into the vector space 11. The vector registers each have a capacity of N vector elements, each element is separately addressable. If concatenation of the initial contents of a base and offset address register sums to the address of vector register 1, element 1, that element may be addressed. If thereafter, the contents of the offset register is incremented, vector register 1, element 2 may be accessed. As will be described, the embodiment of the invention illustrated herein uses a single offset register, and two base registers to successively access successive elements of two vector register operands by incrementing the offset register only after the selected elements of both vectors have been accessed. Thus, with the offset register at a particular value, corresponding elements of two vectors are accessible, as illustrated in FIG. 4.

DEPR:
A second vector may be accessed using the contents of VR2 49 (coupled to gate 43), for example, and the identical offset register. Of course, under these circumstances the offset register is incremented only after accessing the associated element of the second vector operand in sequence.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 12. Document ID: US 4442519 A

L13: Entry 12 of 15 File: USPT Apr 10, 1984

DOCUMENT-IDENTIFIER: US 4442519 A
TITLE: Memory address sequence generator

ABPL:
Apparatus consisting of combinations of interconnected logic elements for generating preselected sequences of addresses for the listing of a matrix memory as a function of preset constants and variable timing impulses, wherein there are first and second X and Y address generators with controlled selection means for selecting the first or the second of the X and Y address pairs, each of the address generators being settably controllable to generate a preselected sequence of addresses in ascending or descending order, with settable increments within the sequence, settable masking, and settable displacements from a fixed reference origin.

DEPR:
The home and away feature need not be confined to individual cell sequences, but may also be used to test corresponding areas of a memory which share sense amplifiers. The home and away addresses would then follow the same sequence, having identical incremental values, masking and cycle counting controls but differ only in their offsets. Alternate home and away addressing would test a succession of cells occupying the same relative positions with respect to two different geometric areas of the memory.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 13. Document ID: US 4386614 A

L13: Entry 13 of 15 File: USPT Jun 7, 1983

DOCUMENT-IDENTIFIER: US 4386614 A
TITLE: System for comparing a real-time waveform with a stored waveform

ABPL:
A system for storing time-varying kinesiograph waveforms and continuously displaying the stored waveforms on the screen of a cathode-ray tube (CRT). In a recording mode, the waveforms are periodically sampled, digitized, and then stored in a block of random access memory reserved for that waveform. In a display mode, the Y axis of the CRT is driven by a digital-to-analog converter which receives digitized samples from the memory block corresponding to the displayed waveform. The X axis of the CRT is driven by a second digital-to-analog converter, which, in an X-Y mode, also receives digitized samples from a selected block of memory. In a sweep mode, the X axis digital-to-analog converter receives the continuously incrementing memory addresses, which read out digitized samples from the memory block for the displayed waveform. The system may also display an expanded portion of a waveform in the sweep mode by incrementing the memory address from one of several predetermined values. In the X-Y mode, two pairs of kinesiograph waveforms may be displaced with respect to each other on the left and righthand sides of the CRT screen. A multiplexer for the X and Y axes allows a real-time kinesiograph waveform to be superimposed on the same stored waveform to facilitate mandibular movement comparisons. The system may also operate in a sensor positioning mode in which a line connecting the optimum position of the sensors and the current position of the sensors is generated on the screen of the CRT.

DEPR:
In the event that only EMG signals are found to be present at 642, the peak detection subroutine is called at 652, an appropriate offset is added and the resulting signal stored in memory at 654, and the storage counter is incremented at 656.

DEPR:
Returning now to decision block 630, if the mode switch 34 is found to be in the fast sweep mode, the program branches to 680, where the characteristic of the inputs is determined. If only MKG (kinesiograph) signals are present, the MKG's inputs are sampled at 682, the offset is added and the result stored in memory 684, and the storage counter is incremented at 686. In the event that the incoming signals are not MKG signals only, the program branches to 688 to determine whether only EMG signals are present. If such is the case, the EMG inputs are sampled at 690, the offset is added to the samples and the result stored in memory at 692, and the storage counter is incremented at 694. Finally, if the incoming signals are found to consist of both MKG and EMG data, four MKG and four EMG channels are sampled at 696, an offset is added to the samples and the result stored in memory at 698, and the storage counter is incremented at 700.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 14. Document ID: US 4336466 A

L13: Entry 14 of 15 File: USPT Jun 22, 1982

DOCUMENT-IDENTIFIER: US 4336466 A
TITLE: Substrate bias generator

ABPL:
A substrate bias generator for an integrated circuit, metal-oxide-semiconductor (MOS) random access memory (RAM) is described. The on-chip generator includes two input terminals for receiving first and second trains of periodic pulses. The periodic pulses have the same frequency and are phase synchronized. However, the first train of pulses has a greater duty cycle than the second train of pulses. Amplitude transitions associated with the first and second trains of pulses are capacitively coupled to first and second nodes, respectively. A pair of transistors are coupled to the nodes, one transistor for clamping the first node to ground when the second node receives a positive-going voltage transition, and another transistor for selectively coupling amplitude transitions from the first node to the second node. In operation, both nodes are driven more negative with each successive incoming pulse until they reach about -5 volts for the case in which the amplitude of the incoming pulses is 5 volts. A third transistor closes a current path between the first node and the chip's substrate when the substrate voltage is at least one threshold voltage more positive than the first node voltage. As a result, the substrate voltage is driven to a negative level which is about one threshold voltage more positive than the furthest negative voltage level on the first node.

DEPR:
Enhancement mode transistor 27 is connected between node or junction 28 and substrate 16 for activation whenever the potential of node 28 is more than the threshold voltage of transistor 27 below the potential of substrate 16. When transistor 27 is turned on, current flows between the substrate 16 and node 28 so that the potential on substrate 16 is within one threshold voltage of the negative potential on node 28. Over a period of time, the negative potential on node 28 is incremently coupled down to a negative voltage limit which is directly proportional to the amplitude transitions at the input terminals. Consequently, the potential on substrate 16 is incrementally biased to a lower negative potential until the substrate 16 reaches a negative voltage which is offset above the negative voltage at node 28 only by the threshold voltage of transistor 27. Thereafter, this negative voltage on substrate 16 is substantially maintained. Any change in substrate voltage due to leakage is compensated for during the following pumping cycle which is described in detail below.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 15. Document ID: US 3878983 A

L13: Entry 15 of 15 File: USPT Apr 22, 1975

DOCUMENT-IDENTIFIER: US 3878983 A
TITLE: System for numerical control of a machine tool

ABPL:
A system in which a machine tool is controlled by a digital computer and an operator to perform a sequence of machining operations. In a programming mode, the machine tool cutting element is positioned by an operator relative to an object to be machined. The relative position of the cutting element is adjusted so that the cutting element passes through a sequence of spatial points at which a subsequent machining operation is desired. In association with each point, a sequence of digital signals is generated in a programming mode in response to an operator directive and that sequence is stored in a digital computer memory. Subsequently, in a machining mode, stored sequence is translated to a machine tool control signal which drives the machine tool. An operator may direct the digital computer in an editing mode to select ones or groups of the stored sequences and to modify those selected sequences. The operator may also direct the computer in the machining mode to generate the corresponding control signals for selected ones or groups of the stored sequences so that the corresponding machining operations are performed.

DEPR:
In response thereto, computer 30 selects the last two X-Y SEQUENCES in the previously stored program, stores those SEQUENCES at temporary storage locations in memory 34, and determines the x and y change data from the difference in the x and y coordinate data from those last two X-Y SEQUENCES, i.e., the x and y change data is dependent upon the last two X-Y SEQUENCES. Computer 30 then modifies the x and y coordinate data stored with the last SEQUENCE at the temporary storage location in one of the following ways: if only the repeat last x increment control 137 was activated by the operator, the x coordinate data are offset by the amount of the x change data; if only the repeat last y control 138 was activated, the y coordinate data are offset by the amount of the y change data; and if both controls 137 and 138 were activated, both the x and y coordinate data are changed by the respective x and y change data. The modified version of the last X-Y SEQUENCE as stored at the temporary location of memory 35 is added to the next available SEQUENCE location in the stored program portion of memory 35.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Drawi Desc | Image

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Term	Documents
INCREMENT$	0
INCREMENT.USPT.	62895
INCREMENTA.USPT.	4
INCREMENTABILITY.USPT.	2
INCREMENTABLE.USPT.	181
INCREMENTABLE-TYPE.USPT.	1
INCREMENTABLE/DECREMENTABLE.USPT.	2
INCREMENTABLY.USPT.	17
INCREMENTAELLY.USPT.	1
INCREMENTAI.USPT.	1
(L10 AND ((INCREMENT$) WITH (OFFSET$) WITH ONLY)).USPT.	15

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